STATEMENT UNDER 37 CFR § 3.73(b)
ESTABLISHMENT OF ASSIGNEE

Applicant	:	Bartlomiej Pawlak, et al.
App. No.	:	10/596612
Filed	:	6/19/2006
For	:	SEMICONDUCTOR SUBSTRATE WITH SOLID PHASE EPITAXIAL REGROWTH WITH REDUCED JUNCTION LEAKAGE AND METHOD OF PRODUCING SAME
Examiner	:	Alexander G. Ghyka
Group Art Unit	:	2812

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This document is being filed with a copy of a Power of Attorney signed by the Assignee. This Statement sets forth the chain of title of the above-identified application.

IMEC, is the Assignee of the entire right, title, and interest of the above-referenced application by virtue of:

A chain of title, in reverse order, from the inventor(s) to the current Assignee as shown by the following recorded assignments:

1. The attached copy of the Assignment being forwarded to the Recordation Branch concurrently under separate cover.
2. Assignment from Koninklijke Philips Electronics N.V. to NXP B.V. recorded in the United States Patent and Trademark Office on August 17, 2007, at Reel 019719, and Frame 0843.
3. Assignment from Bartlomiej Jan Pawlak, Raymond James Duffy and Richard Lindsay to Koninklijke Philips Electronics N.V. recorded in the United States Patent and Trademark Office on June 19, 2006, at Reel 017806, and Frame 0712.

The undersigned is an agent of Customer Number 20995 and is authorized to act on behalf of the Assignee. Please recognize or change the correspondence address for the above-identified application to **Customer No. 20995.**

Respectfully submitted,
KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 2/2/12

By: _____
John M. Carson
Registration No. 34,303
Attorney of Record
Customer No. 20995
(858) 707-4000

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ASSIGNMENT

WHEREAS, NXP B.V., a Dutch corporation having offices at High Tech Campus 60, 5656 AG Eindhoven, Netherlands (hereinafter "ASSIGNOR"), represents and warrants that it is the sole owner of the entire right, title, and interest to certain new and useful improvements for which ASSIGNOR has filed United States issued Letters Patents and applications for Letters Patents in the United States (hereinafter "the Patents and Patent Applications") identified in the attached Exhibit A.

WHEREAS, IMEC, a Belgian corporation having offices at Kapeldreef 75, 3001 Leuven, Belgium (hereinafter "ASSIGNEE") desires to purchase the entire right, title, and interest in and to the inventions disclosed in the Patents and Patent Applications;

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, ASSIGNOR hereby further acknowledges that it has sold, assigned, and transferred, and by these presents does hereby sell, assign, and transfer, unto ASSIGNEE, its successors, legal representatives, and assigns, the entire right, title, and interest throughout the world in, to, and under the said Improvements, and the said Patents and Patent Applications and all Patents that may be granted thereon, and all provisional applications relating thereto, and all divisions, continuations, reissues, reexaminations, renewals, and extensions thereof, and all rights of priority under International Conventions and applications for Letters Patent that may hereafter be filed for said improvements or for the said Patents and Patent Applications in any country or countries foreign to the United States; and ASSIGNOR hereby authorizes and requests the Commissioner of Patents of the United States, and any Official of any country foreign to the United States, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patents for said Improvements and all Letters Patents resulting from the Patents and Patent Applications to ASSIGNEE, its successors, legal representatives, and assigns, in accordance with the terms of this Agreement.

ASSIGNOR does hereby sell, assign, transfer, and convey to ASSIGNEE, its successors, legal representatives, and assigns all claims for damages and all remedies arising out of any violation of the rights assigned hereby that may have accrued prior to the date of assignment to ASSIGNEE, or may accrue hereafter, including, but not limited to, the right to sue for, collect, and retain damages for past infringements of the Letters Patents before or after issuance;

ASSIGNOR hereby covenants and agrees that it will communicate to ASSIGNEE, its successors, legal representatives, and assigns any facts known to ASSIGNOR respecting the Patents and Patent Applications immediately upon becoming aware of those facts, and that it will testify in any legal proceeding involving any of the Patents and Patent Applications, will sign all lawful papers, execute all divisional, continuing, and reissue applications, make all rightful oaths, and will generally do everything possible to aid ASSIGNEE, its successors, legal representatives, and assigns to obtain and enforce the Patents and Patent Applications in all countries.

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 25th day of January, 2012

NXP B.V.

By: Marc M Schuurten

Name Printed: Marc M. Schuurtes

Title: Head IP Creation & Strategy

Date: _____

Witnessed by: _____

Printed Name: Johanna Noreby - Defesche

COPY
-DO NOT RECORD-

Exhibit A

NXP Patent Family	IMEC reference	Title	Filing Date	Application No.
001288	2007/034	SEMICONDUCTOR DEVICE HAVING A POLYSILICON ELECTRODE INCLUDING AMORPHIZING, RECRYSTALLISING, AND REMOVING PART OF THE POLYSILICON ELECTRODE	11/14/2008	11/917103
GB040113	2009/223	PLANAR DUAL GATE SEMICONDUCTOR DEVICE	11/22/2006	11/597816
GB040126	2007/141	SEMICONDUCTOR ON INSULATOR SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE	7/9/2010	11/629419
NL030079	2003/045	METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE OBTAINED BY MEANS OF SUCH A METHOD	8/3/2005	10/544412
NL030081	2003/047	METHOD OF MANUFACTURING MOS TRANSISTORS WITH GATE ELECTRODES FORMED IN A PACKET OF METAL LAYERS DEPOSITED UPON ONE ANOTHER	8/3/2005	10/544413
NL030347	2003/048	GATE ELECTRODE FOR SEMICONDUCTOR DEVICES	9/22/2005	10/550741
NL030623	2003/020	FORMATION OF JUNCTIONS AND SILICIDES WITH REDUCED THERMAL BUDGET	11/30/2005	10/559069
NL031072	2003/069	METHOD OF FABRICATING A DOUBLE GATE FIELD EFFECT TRANSISTOR DEVICE, AND SUCH A DOUBLE GATE FIELD EFFECT TRANSISTOR DEVICE	3/1/2006	10/570478
NL031259	2003/079	SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SUCH A SEMICONDUCTOR DEVICE	4/11/2006	10/575288
NL031497	2007/134	METHOD FOR FORMING A STRAINED SI-CHANNEL IN A MOSFET STRUCTURE	6/13/2006	10/596422
NL031498	2004/089	SEMICONDUCTOR SUBSTRATE WITH SOLID PHASE EPITAXIAL REGROWTH WITH REDUCED JUNCTION LEAKAGE AND METHOD OF PRODUCING SAME	6/19/2006	10/596612
NL031500	2004/080	SEMICONDUCTOR SUBSTRATE WITH SOLID PHASE EPITAXIAL REGROWTH WITH REDUCED DEPTH OF DOPING PROFILE AND METHOD OF PRODUCING SAME	4/24/2009	10/596603

NXP Patent Family	IMEC reference	Title	Filing Date	Application No.
NL040276	2004/076	FIELD EFFECT TRANSISTOR AND METHOD OF MANUFACTURING A FIELD EFFECT TRANSISTOR	9/11/2006	10/598755
NL040280	2004/078	METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE INCLUDING DOPANT INTRODUCTION	9/11/2006	10/598744
NL040928	2007/137	METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SUCH A SEMICONDUCTOR DEVICE	3/6/2009	11/574338
NL040929	2007/138	SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THEREOF	10/8/2007	11/574341
NL041040	2007/135	SEMICONDUCT DEVICE AND METHOD OF MANUFACTURING SUCH A SEMICONDUCTOR DEVICE	11/12/2007	11/574245
BE020043	2003/039	METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE OBATINED WITH SUCH A METHOD	6/16/2005	10/539224